

What Is Claimed Is:

1        1. A method for forming a transistor array on a substrate,  
2        comprising the steps of:

3        forming on the substrate a plurality of signal lines along  
4        a first direction and a plurality of gate lines along a second  
5        direction to define a plurality of pixels, the first direction  
6        being perpendicular to the second direction, each pixel  
7        including a first area;

8        forming a switching unit in the first area of each pixel;

9        forming a first photoresist layer to cover a first group of  
10       the pixels;

11       forming a second photoresist layer to cover a second group  
12       of the pixels; and

13       forming a third photoresist layer to cover a third group of  
14       the pixels,

15       wherein the first area of each pixel is covered by at least  
16       two of the first, second and third photoresist layers.

1        2. The method of claim 1 wherein the switching units are thin  
2        film transistors, and the method further comprises a step of  
3        forming a through hole in at least two of the first, second and  
4        third photoresist layers within each first area so as to expose  
5        each drain electrode of each thin film transistor.

1        3. The method of claim 2, further comprising a step of  
2        forming a conducting layer on the first, second and third  
3        photoresist layers, wherein the conducting layer connects to  
4        each drain electrode of each thin film transistor via its  
5        corresponding through hole.

1       4. The method of claim 1, further comprising a step of  
2 forming a passivation layer between the first photoresist layer  
3 and the switching units.

1       5. The method of claim 4 in which the switching units are  
2 thin film transistors, further comprising a step of forming a  
3 plurality of through holes in at least two of the first, second,  
4 and third photoresist layers and the passivation layer so as to  
5 expose drain electrodes of the thin film transistors therein.

1       6. The method of claim 5, further comprising a step of  
2 forming a conducting layer on the first, second and third  
3 photoresist layers, and the conducting layer being connected to  
4 each drain electrode via each corresponding through hole in the  
5 first area.

1       7. A panel of a flat panel display, comprising:  
2       a glass substrate;  
3       a plurality of signal lines disposed on the glass substrate  
4 along a first direction and a plurality of gate lines disposed  
5 on the glass substrate along a second direction to define a  
6 plurality of pixels, the first direction being perpendicular to  
7 the second direction, each pixel including a first area;  
8       a plurality of switching units disposed in the first areas  
9 of the pixels;  
10      a first photoresist layer covering a first group of the  
11 pixels;  
12      a second photoresist layer covering a second group of the  
13 pixels; and

14        a third photoresist layer covering a third group of the  
15 pixels,

16        wherein the first area of each pixel is covered by at least  
17 two of the first, second and third photoresist layers.

1        8. The panel of claim 7 wherein the switching units are thin  
2 film transistors, and, in each first area, the panel further  
3 comprises a plurality of through holes in at least two of the  
4 first, second and third photoresist layers so as to expose each  
5 drain electrode of each thin film transistor therein.

1        9. The panel of claim 8, further comprising a conducting  
2 layer formed on the first, second and third photoresist layers  
3 and connected to each drain electrode via each corresponding  
4 through hole in the first area.

1        10. The panel of claim 7, further comprising a passivation  
2 layer formed between the first photoresist layer and each  
3 switching unit in each first area.

1        11. The panel of claim 10 wherein the switching units are  
2 thin film transistors, and the substrate further comprises a  
3 plurality of through holes in at least two of the first, second  
4 and third photoresist layers and the passivation layer so as to  
5 expose drain electrodes of the thin film transistors.

1        12. The panel of claim 11, further comprising a conducting  
2 layer formed on the first, second and third photoresist layers,

3 and connected to each drain electrode via each through hole in  
4 each first area.

1       13. A flat panel display, comprising:  
2        a first substrate;  
3        a second substrate facing the first substrate;  
4        a liquid crystal layer disposed between the first substrate  
5 and the second substrate;  
6        a plurality of signal lines disposed on the first substrate  
7 along a first direction and a plurality of gate lines disposed  
8 on the glass substrate along a second direction to define a  
9 plurality of pixels, the first direction being perpendicular to  
10 the second direction, each pixel having a first area;  
11       a plurality of switching units disposed in the first areas  
12 of the pixels;  
13       a first photoresist layer covering a first group of the  
14 pixels;  
15       a second photoresist layer covering a second group of the  
16 pixels; and  
17       a third photoresist layer covering a third group of the  
18 pixels,  
19       wherein the first areas of each pixel is covered by at least  
20 two of the first, second and third photoresist layers.

1       14. The display of claim 13 wherein the switching units are  
2 thin film transistors, and the display further comprises a  
3 plurality of through holes formed in at least two of the first,  
4 second and third photoresist layers so as to expose drain  
5 electrodes of the thin film transistors therein.

1        15. The display of claim 14, further comprising a conducting  
2        layer formed on the first, second and third photoresist layers  
3        and connected to each drain electrode via its corresponding  
4        through hole in the first areas.

1        16. The display of claim 13, further comprising a  
2        passivation layer formed between the first photoresist layer and  
3        the switching units.

1        17. The display of claim 16 wherein the switching units are  
2        thin film transistors, and the display further comprises a  
3        plurality of through holes formed in at least two of the first,  
4        second and third photoresist layers and the passivation layer  
5        so as to expose drain electrodes of the thin film transistors  
6        therein.

1        18. The display of claim 17, further comprising a conducting  
2        layer formed on the first, second and third photoresist layers  
3        and connected to each drain electrode via its corresponding  
4        through hole.